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10/816,853	04/05/2004	Shigeru Yagi	119349	1813

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EXAMINER	
MONBLEAU, DAVIENNE N	
ART UNIT	**PAPER NUMBER**
2878	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,853	YAGI ET AL.	
	Examiner	Art Unit	
	Davienne Monbleau	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment filed on 1/17/06 has been entered. Claims 1, 7, 13, 15, and 21 have been amended. New claims 22 and 23 have been added. Claims 1-23 are pending.

Response to Arguments

Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

The drawings were received on 1/17/06. These drawings are accepted.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-5, 7-14, and 22 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4, 7, 12, and 14 of copending Application No. 10/817,939 in view of Hashimoto (U.S. 6,340,606).

This is a provisional obviousness-type double patenting rejection.

Regarding claim 1, *'939* teaches (claim 1) a light detection device comprising: a light-receiving element including a semiconductor layer for detecting light (line 2) and a first electrode which is electrically connected with the semiconductor layer Line 3); an insulative substrate for supporting the light-receiving element (line 5); and a second electrode which is provided so as to be exposed at a first face and a second face of the insulative substrate (lines 6-7) wherein the light-receiving element is disposed on the first face of the insulative substrate, and the first electrode is electrically connected with the second electrode that is exposed at the first face of the insulative substrate (lines 11-13). *'939* does not teach that the second electrode extends through the insulative substrate. *Hashimoto* teaches (Figure 5) a semiconductor device packaging structure comprising a semiconductor element (32), an insulative substrate (34) for supporting the semiconductor element (32), and a second electrode (36) extending through the insulative substrate (34), wherein the semiconductor element (32) is disposed on the first face of the insulative substrate (34), and the first electrode (33) is electrically connected with the second electrode (36) that is provided at the at least a part of the first face of the insulative substrate (34). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the electrode structure taught by *Hashimoto* in *'939* to have a packaging device appropriate for high-density mounting that can avoid cracks in external electrodes.

Regarding claim 2, *'939* as modified by *Hashimoto* teaches (*'939*, claim 2) that the first electrode is constituted by at least two electrodes, and the second electrode is constituted by at least two electrodes.

Regarding claim 3, *'939* as modified by *Hashimoto* teaches (*'939*, claim 3) that the second electrode comprises a metal electrode.

Regarding claim 4, *'939* as modified by *Hashimoto* teaches (*'939*, claim 4) that the insulative substrate absorbs visible light.

Regarding claim 5, *'939* as modified by *Hashimoto* teaches (*'939*, claim 1, lines 3-4) that the light-receiving element includes a transparent substrate on which the semiconductor layer and the first electrode are disposed.

Regarding claim 7, *'939* as modified by *Hashimoto* teaches (*'939*, claim 12) that the first electrode is connected with the second electrode that is exposed at the first face of the insulative substrate via a conductive member.

Regarding claim 8, *'939* as modified by *Hashimoto* teaches (*'939*, claim 12) that excluding a portion that is connected by the conductive member, at least a portion of a face of the light-receiving element which face opposes the insulative substrate is fixed to the insulative substrate. It is obvious that some type of adhesive must be used in order to fix the light-receiving element to the substrate.

Regarding claim 9, *'939* as modified by *Hashimoto* (*'939*, claim 1) teaches an insulative substrate but does not teach that a recess portion is formed in the insulative substrate. It would have been obvious, however, to one of ordinary skill in the art at the time of the invention to use a particular substrate shape to optimize the overall stability and compactibility of the device.

Regarding claim 10, *'939* as modified by *Hashimoto* teaches (*'939*, claim 7) that the semiconductor layer of the light-receiving element comprises a nitride including nitrogen and at least one element selected from the group consisting of Al, Ga and In.

Regarding claims 11 and 12, *'939* as modified by *Hashimoto* teach (*'939*, claims 1 and 7) a semiconductor layer but does not teach the specific material composition. It would have been obvious, however, to one of ordinary skill in the art at the time of the invention to use particular semiconductor materials and elements in *Hsieh* as modified by *Hashimoto* since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. Materials have specific inherent characteristics that determine which wavelengths will be absorbed and/or transmitted, thus defining the wavelength range of the detector.

Regarding claim 13, *'939* as modified by *Hashimoto* teaches (*'939*, claims 1 and 14) that the second face is a face corresponding to an opposite face with respect to the first face of the insulative substrate.

Regarding claim 14, *'939* as modified by *Hashimoto* teaches (*'939*, claim 1) a semiconductor light-receiving element (34), but does not teach a plurality of light-receiving elements. It would have been obvious, however, to one of ordinary skill in the art at the time of the invention to use a plurality of light-receiving elements to adjust a number of different operating characteristics, such as increasing the incident light area, detecting different wavelengths/detector, or increase the intensity.

Regarding claim 22, *'939* as modified by *Hashimoto* teaches (*'939*, claim 1 and *Hashimoto*, Figure 5) that the second electrode (36) is formed through a through-hole (34a) provided in the insulative substrate (34).

Claims 15-21 and 23 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4, 7, and 14 of copending Application No. 10/817,939 in view of Hashimoto (U.S. 6,340,606) and Hsieh et al. (U.S. 6,649,834).

Regarding claim 15, *'939* teaches (claim 1) a light detection device mounting method comprising preparing a light-receiving element (line 2) which includes a first electrode (line 3) which is electrically connected to the light-receiving element, providing a second electrode (line 6) so as to be exposed at a first face and a second face of an insulative substrate, and preparing the light detection device by disposing the light-receiving element on the first face of the insulative substrate (line 11-13) such that the first electrode is electrically connected with the second electrode that is exposed at the first face of the insulative substrate. *'939* does not teach that the second electrode extends through the insulative substrate. *Hashimoto* teaches (Figure 5) a semiconductor device packaging structure comprising a semiconductor element (32), an insulative substrate (34) for supporting the semiconductor element (32), and a second electrode (36) extending through the insulative substrate (34), wherein the semiconductor element (32) is disposed on the first face of the insulative substrate (34), and the first electrode (33) is electrically connected with the second electrode (36) that is provided at the at least a part of the first face of the insulative substrate (34). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the electrode structure taught by *Hashimoto* in *'939* to

have a packaging device appropriate for high-density mounting that can avoid cracks in external electrodes. *'939* does not teach that surface-mounting the light detection device on a circuit board such that the second electrode that is provided at the at least a part of the second face of the insulative substrate is connected with an external terminal of the circuit board. *Hsieh* teaches (Figure 2) a light detection device mounting method comprising preparing a light-receiving element (34) which includes a first electrode (56), providing a second electrode (30) so as to be exposed at a first face and a second face of an insulative substrate (32), and surface-mounting the light detection device on a circuit board (51) such that the second electrode (30) that is exposed at the second face of the insulative substrate (32) is connected with an external terminal of the circuit board (51). It would have been obvious to one of ordinary skill in the art at the time of the invention to surface-mount the light detection device of *'939* onto a circuit board, as taught by *Hseih*, to facilitate electrical connections to a plurality of devices.

Regarding claim 16, *'939* as modified by *Hashimoto* and *Hseih* teaches ('939, claim 2) that the first electrode is constituted by at least two electrodes, and the second electrode is constituted by at least two electrodes.

Regarding claim 17, *'939* as modified by *Hashimoto* and *Hseih* teaches ('939, claim 3) that the second electrode comprises a metal electrode.

Regarding claim 18, *'939* as modified by *Hashimoto* and *Hseih* teaches ('939, claim 4) that the insulative substrate absorbs visible light.

Regarding claim 19, *'939* as modified by *Hashimoto* and *Hseih* teaches ('939, claim 1) that the light-receiving element includes a transparent substrate on which the semiconductor layer and the first electrode are disposed.

Regarding claim 20, *'939* as modified by *Hashimoto* and *Hseih* teaches ('939, claim 7) that the semiconductor layer of the light-receiving element comprises a nitride including nitrogen and at least one element selected from the group consisting of Al, Ga and In.

Regarding claim 21, *'939* as modified by *Hashimoto* and *Hseih* teaches ('939, claims 1 and 14) that the second face is a face corresponding to an opposite face with respect to the first face of the insulative substrate.

Regarding claim 23, *'939* as modified by *Hashimoto* and *Hseih* teaches (*'939*, claim 1 and *Hashimoto*, Figure 5) that the second electrode (36) is formed through a through-hole (34a) provided in the insulative substrate (34).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3, 5-17, and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh et al. (U.S. 6,649,834) in view of Hashimoto (U.S. 6,340,606).

Regarding Claim 1, *Hsieh* teaches in Figure 2 a light detection device comprising a light-receiving element (34) and a first electrode (56) which is electrically connected with the light-receiving element (34), an insulative substrate (32) for supporting the light-receiving element (34), and a second electrode (30) which is provided so as to be exposed at a first face and a second face of the insulative substrate (32), wherein the light-receiving element (34) is disposed on the first face of the insulative substrate (32), and the first electrode (56) is electrically connected with the second electrode (30) that is exposed at the first face of the insulative substrate (32). *Hsieh* teaches an image sensor but does not teach the type of image sensor (i.e. semiconductor.) It would have been obvious, however, to one of ordinary skill in the art at the time of the invention to use a semiconductor light-receiving element, which would comprise a semiconductor layer, because semiconductor detectors are often used as image sensors (i.e. CMOS detector arrays) and require stable, insulated packaging. *Hsieh* does not teach that the second electrode extends through the insulative substrate. *Hashimoto* teaches (Figure 5) a semiconductor device packaging structure comprising a semiconductor element (32), an insulative substrate (34) for supporting the semiconductor element (32), and a second electrode (36) which is provided at at least a part of a first face and at least a part of a second face of the insulative substrate (34), the second electrode (36) extending through the insulative substrate (34), wherein the semiconductor element (32) is disposed on the first face of the insulative substrate (34), and the first electrode (33) is electrically connected with the second electrode (36) that is provided at the at least a part of the first face of the insulative substrate (34). It would

have been obvious to one of ordinary skill in the art at the time of the invention to use the electrode structure taught by *Hashimoto* in *Hsieh* to have a packaging device appropriate for high-density mounting that can avoid cracks in external electrodes.

Regarding Claim 15, *Hsieh* teaches in Figure 2 a light detection device mounting method comprising preparing a light-receiving element (34) which includes a first electrode (56) which is electrically connected to the light-receiving element (34), providing a second electrode (30) so as to be exposed at a first face and a second face of an insulative substrate (32), preparing the light detection device by disposing the light-receiving element (34) on the first face of the insulative substrate (32) such that the first electrode (56) is electrically connected with the second electrode (30) that is exposed at the first face of the insulative substrate (32), and surface-mounting the light detection device on a circuit board (51) such that the second electrode (30) that is exposed at the second face of the insulative substrate (32) is connected with an external terminal of the circuit board (51). *Hsieh* teaches an image sensor but does not teach the type of image sensor (i.e. semiconductor.) It would have been obvious, however, to one of ordinary skill in the art at the time of the invention to use a semiconductor light-receiving element, which would comprise a semiconductor layer, because semiconductor detectors are often used as image sensors (i.e. CMOS detector arrays) and require stable, insulated packaging. *Hsieh* does not teach that the second electrode extends through the insulative substrate. *Hashimoto* teaches (Figure 5) a semiconductor device packaging structure comprising a semiconductor element (32), an insulative substrate (34) for supporting the semiconductor element (32), and a second electrode (36) which is provided at at least a part of a first face and at least a part of a second face of the insulative substrate (34), the second electrode (36) extending through the insulative

substrate (34), wherein the semiconductor element (32) is disposed on the first face of the insulative substrate (34), and the first electrode (33) is electrically connected with the second electrode (36) that is provided at the at least a part of the first face of the insulative substrate (34). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the electrode structure taught by *Hashimoto* in *Hsieh* to have a packaging device appropriate for high-density mounting that can avoid cracks in external electrodes.

Regarding Claims 2 and 16, *Hsieh* as modified by *Hashimoto* teaches (*Hsieh*: Figure 2) that the first electrode (56) is constituted by at least two electrodes and the second electrode (30) is constituted by at least two electrodes.

Regarding Claims 3 and 17, *Hsieh* as modified by *Hashimoto* teaches (*Hsieh*: Figure 2) that the second electrode (30) comprises a metal electrode.

Regarding Claims 5 and 19, *Hsieh* as modified by *Hashimoto* teaches (*Hsieh*: Figure 2) a transparent substrate (38) above the light-receiving element (34) and the first electrode (56).

Regarding Claim 6, *Hsieh* as modified by *Hashimoto* teaches (*Hsieh*: Figure 2) that the light-receiving element (34) comprises a transparent substrate (38) but does not teach that the first electrode (56) comprises a first layer and a second layer, and the first layer, the semiconductor layer and the second layer are laminated on the transparent substrate in this order, and the first layer of the first electrode is transparent. It would have been obvious, however, to one of ordinary skill in the art at the time of the invention to alter the electrode configuration in *Hsieh* to accommodate other housing arrangements, which may then require using transparent electrodes.

Regarding Claim 7, *Hsieh* as modified by *Hashimoto* teaches (*Hashimoto*: Figure 5) that the first electrode (33) is connected with the second electrode (36) that is exposed at the first face of the insulative substrate (34) via a conductive member (40).

Regarding Claim 8, *Hsieh* as modified by *Hashimoto* teaches (*Hsieh*: Figure 2) 2 that excluding a portion that is connected by the conductive member (36), at least a portion of a face of the light-receiving element (34) which face opposes the insulative substrate (32) is fixed to the insulative substrate (32) with an adhesive layer there between (49). (See column 3 lines 29-31.)

Regarding Claim 9, *Hsieh* as modified by *Hashimoto* teaches (*Hsieh*: Figure 2) a recess portion is formed in the insulative substrate (32) and the light-receiving element (34) is embedded in the recess portion.

Regarding Claims 10-12 and 20, see discussion on Claims 1 and 15. It would have been obvious to one of ordinary skill in the art at the time of the invention to use particular semiconductor materials and elements in *Hsieh* as modified by *Hashimoto* since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. Materials have specific inherent characteristics that determine which wavelengths will be absorbed and/or transmitted, thus defining the wavelength range of the detector.

Regarding Claims 13 and 21, *Hsieh* as modified by *Hashimoto* teaches (*Hsieh*: Figure 2) that the second face is a face corresponding to an opposite face with respect to the first face of the insulative substrate (32).

Regarding Claim 14, *Hsieh* as modified by *Hashimoto* teaches a semiconductor light-receiving element (34), but does not teach a plurality of light-receiving elements. It would have

been obvious, however, to one of ordinary skill in the art at the time of the invention to use a plurality of light-receiving elements to adjust a number of different operating characteristics, such as increasing the incident light area, detecting different wavelengths/detector, or increase the intensity.

Regarding claims 22 and 23, *Hsieh* as modified by *Hashimoto* teaches (*Hashimoto*: Figure 5) that the second electrode (36) is formed through a through-hole (34a) provided in the insulative substrate (34).

Claims 4 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh in view of Hashimoto, as applied to claims 1 and 15 above, respectively, and in further view of Oyoshi et al. (JP 7-38138).

Regarding Claims 4 and 18, *Hsieh* as modified by *Hashimoto* teaches (*Hsieh*: Figure 2) an image sensor (34) but does not teach the desired wavelength detection range. *Oyoshi* teaches in the abstract a UV sensor comprising a substrate that absorbs visible light. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a substrate that absorbs visible light in *Hsieh*, as taught by *Oyoshi*, to lessen the detector sensitivity to undesired wavelengths, for example visible light, when the detector is a UV detector.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Davienne Monbleau whose telephone number is 571-272-1945. The examiner can normally be reached on Monday through Friday 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 571-272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Davienne Monbleau

DNM

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